**CHAPTER 2**

**LITERATURE SURVEY**

**2.1 INTRODUCTION**

This chapter includes all the reference papers. Objective, concepts and experimental results of each paper are presented. Advantages and drawbacks of each paper are discussed.

**2.2 PAPER 1**

**Title:**Arash Azizi Mazreah, Mohammad Noorollahi Romani, Mohammad Taghi Manzuri, Ali Mehrparvar, *“A low power and high density cache memory on novel SRAM cell”*, IEICE Electronics Express, Vol.6, August 2009

**2.2.1 OBJECTIVE**

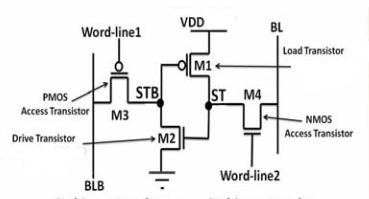
The objective is to develop an SRAM cell with four transistors to reduce the cell area size and power consumption with no performance degradation.

**2.2.2 INTRODUCTION**

Conventional SRAMs that use 6T SRAM cells have difficulty in meeting the growing demand for a larger memory capacity in mobile applications. Furthermore, in a conventional SRAM cell one of the two bit-lines must be discharged regardless of the written value. Therefore the power consumption in writing both “0” and “1” are the same. Also during the read operation one of the two bit-lines must be discharged irrespective of the value stored in the cell. Therefore there are always transitions on bit-lines in both writing “0” and “1” and reading “0” and “1”. Furthermore 6T SRAM cell uses full swing on word-lines and these cause high dynamic power consumption during read and write operations. In response to this requirement an SRAM with 4 transistors is developed. The power consumption of writing and reading zeros in novel cell is much smaller than ones, thus the average power consumption is reduced in caches based on this novel cell.

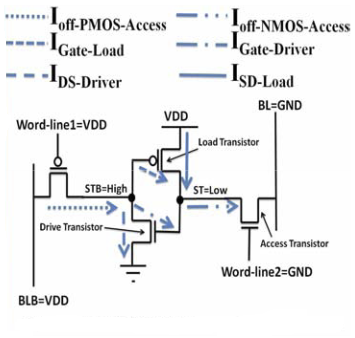
**2.2.3 CELL DESIGN CONCEPT**

Fig (2.1) shows the circuit equivalent to the developed 4T SRAM cell.

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**Fig (2.1) 4T SRAM Cell**

When “1” is stored in the cell, load and drive transistors are ON and there is a positive feedback between ST and STB node. Therefore STB node is pulled to GND by drive transistor and ST node is pulled to VDD by load transistor.

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**Fig (2.2) 4T SRAM Cell in idle mode when “0” is stored**

When “0” is stored in the cell both load and drive transistors are OFF and for data retention without refresh cycle, the following conditions must be satisfied.

IOff-NMOS-access > ISD-Load + IGate-Driver + IGate-Load **Eq (2.1)**

IOff-PMOS-access > IDS-Load + IGate-Driver + IGate-Load **Eq (2.2)**

Fig (2.2) shows leakage current of cell during idle mode for data retention when “0” is stored in the cell. For satisfying the above condition when “0” is stored in the cell we use leakage current of access transistors, especially sub-threshold current of access transistors (IOff-NMOS-access and IOff-PMOS-access ).

To achieve this we can use high threshold voltage for load and drive transistors to reduce sub-threshold currents of these transistors. Low threshold voltage can be used for access transistors; hence leakage current of access transistors will be greater than leakage currents of load and drive transistors. With this threshold voltage assignments above conditions can be satisfied and “0” can be stored in a cell successfully. Leakage currents also depend on the width of the transistors. As width of a transistor increases, leakage currents also increase. As the leakage currents of access transistors should be greater than leakage currents of load and drive transistors, the width of access transistors should be greater than the width of load and drive transistors.

The specifications for 4T SRAM cell are mentioned as follows:

Technology used: 65nm

VDD = 1.2V

(W/L)M1=130nm/65nm­ (W/L)M2=130nm/65nm­

(W/L)M3=260nm/65nm­ (W/L)M4=260nm/65nm­

Normal threshold voltage: VTN = 0.32V VTP = 0.33V

High threshold voltage: VTN = 0.52V VTP = 0.53V

**2.2.4 WRITE AND READ OPERATION**

* **Write operation:** When a write operation is issued the memory cell will go through the following steps.

**1) Bit-line driving:** For a write, data is placed on BL and its compliment is placed on BLB, then WL1 and WL2 are asserted to GND and VDD respectively.

**2) Cell flipping:** This step includes two states as follows.

**(a) When data is logic ‘0’:** In this state, ST node is pulled down to GND by NMOS access transistor STB node will be pulled up to VDD by PMOS access transistor.

**b) When data is logic ‘1’:** In this state, ST node is pulled up to VDD-VTN by NMOS access transistor, and therefore the drive transistor will be ON and STB node will be pulled up to VTP by PMOS access transistor. Load and drive transistors will be ON and positive feedback is created by load and drive transistors between ST and STB nodes.

**3) Idle mode:** At the end of write operation, cell will go to idle mode and WL1 and WL2 are asserted to VDD and GND respectively and BL and BLB return to GND and VDD respectively.

* **Read operation:**

When a read operation is issued the memory cell will go through the following steps.

**1) Bit-line Pre-charging:** For a read, BLB is pre-charged to VDD and then floated. Since, in idle mode BLB maintained at VDD, this step doesn’t include any dynamic energy consumption.

**2) Word-line activation:** In this step WL1is asserted to GND and two states can be considered.

**(a) Stored data is “1”:** When voltage of STB node is low, the voltage of BLB pulled up to low voltage by NMOS access transistor. We refer to this voltage of BLB as VBLB-LOW.

**(b) Stored data is “0”:** When voltage of STB node is high, the voltage of BLB and STB node are equalized. Since in this state, there is very small different between BLB and STB node, power consumption is very small.

**3) Sensing:** After WL1is deactivated, the sense amplifier is enabled to read data on BLB.

**4) Idle mode:** At the end of read operation, cell will go to idle mode and BLB is asserted to VDD.

**2.2.5 LEAKAGE CURRENTS**

4T SRAM cell has to retain its value using leakage currents in one state (when “0” is stored) whereas in another state it retains the data using positive feedback (when “1” is stored). In idle mode when “1” is stored, load and drive transistors are ON thereby creating a positive feedback leakage and access transistors have sub-threshold current. But since load and drive transistors have high threshold voltage, therefore there are paths from supply to ground. Thus leakage current in “1’’ state is greater than that in “0’’ state. Leakage current of 6T SRAM cell when ‘‘0’’ or ‘‘1’’ stored is approximately equal to leakage current of 4T SRAM cell when ‘‘1’’ is stored. Leakage current of 4T SRAM cell when ‘‘0’’ is stored is much smaller than leakage current of 6T SRAM cell when ‘‘0’’ or “1” is stored. Most bits of caches are zeros for both data and instruction streams, so average leakage current is smaller in case of 4T SRAM cache when compared to 6T SRAM cache.

**2.2.6 EXPERIMENTAL RESULTS**

**Dynamic power consumption:**

In idle mode BL and BLB are maintained at GND and VDD, hence there is no transition on bit-lines while writing ‘0’.Hence in 4T SRAM power consumed for writing ‘‘0’’ is smaller than that needed for writing ‘‘1’’, whereas in 6T SRAM both cases consume same power. Further in 4T SRAM cell, when “0” is read from cell, there is no transition on BLB and hence power consumption of reading ‘0’ is smaller than reading “1”. In 6T power consumed for reading and writing “1” is same.

From H-SPICE simulations it is obtained that:

* Power consumption of writing “1” in 4T cell is approximately equal with power consumption of writing “1” or “0” in 6T cell.
* Power consumption of reading “1” or “0” in 4T cell are smaller than power consumption of reading “1” or “0” in 6T cell.
* Average dynamic power consumption of new cell is 40% smaller than that of 6T cell.
* Static power consumption of new cell is 20% less than that of 6T cell.

**Cell area:** The new cell size is 20% smaller than conventional 6T cell size.

**2.2.7 CONCLUSION**

* **Advantages:** Cell area, static power consumption and dynamic power consumption have decreased.
* **Disadvantages:** Delay has increased and SNM has decreased.

**2.3 PAPER 2**

**Title:**

Stefan Cosemans, Wim Dehaene and Francky Catthoor, *“A Low-Power Embedded SRAM for Wireless Applications”*, IEEE Journal of Solid- State circuits, Vol. 42, No. 7, July2007

**2.3.1 OBJECTIVE**

The objective of this paper is to introduce a novel ultra-low-power SRAM in which large power reduction is obtained by the use of four new techniques that allow for a wider and better trade-off between area, delay and active and passive energy consumption.

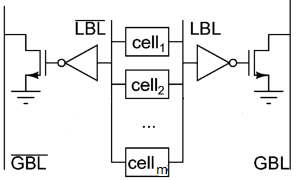
**2.3.2 INTRODUCTION**

Embedded memories play a crucial role in contemporary electronic systems. They are used in different sizes ranging from a few kilobytes for local scratchpads to a few megabytes for on-chip caches. This paper focuses on embedded SRAMs smaller than 1 Mb for use in the lowest levels of the memory hierarchy. Memories at this level of the hierarchy are used very intensively, so their energy consumption has a significant impact on the energy consumption of the entire system. In this paper, a novel SRAM design is introduced. The implemented design techniques consist of a more efficient memory data bus, the exploitation of the dynamic read stability of SRAM cells, a new low-swing write technique and a distributed decoder.

**2.3.3 SHORT BUFFERED BITLINE TECHNIQUE**

In traditional low-power memory designs, the cell read current Iread,cell must create a large enough voltage difference on the bit-lines. Since the bit-line capacitance is very large, this step makes up a large part of the memory access delay. Therefore Iread,cell must be made as large as possible, which results in high cell leakage currents because a large requires large transistor widths, low threshold voltages or a high supply voltage for the cell. Nominal value of Iread,cell is important. Because the cells need to be very small, the intra-die variation of Iread,cell will be large. This requires a large safety margin on the memory delay. Since all cells will remain activated until the slowest cell is ready, this also causes an important increase in energy consumption.

These problems are remedied when the amount of charge that the cell must draw from the bit-line is reduced. Therefore, the bit-line is divided into shorter local bit-lines. Buffer connects local and global bit-lines as shown in fig (2.3).Inverter acts as a sensing element for the buffer. LBL uses a large voltage swing but since capacitance is less, it has limited impact on energy consumption. Buffer consists of a scaled up NMOS transistor. Iread,buffer can be much larger than Iread,cell and suffers less from intra-die variation. Low voltage power supply can be used as pre-charge voltage to the GBL which reduces power consumption.



**Fig (2.3) Buffered Bit-lines**

**Impact on Memory Data bus:**

In traditional designs, amplification at the column level is required to limit Iread,cell impact on memory speed. In buffered bit-line approach, buffer can easily deliver more current so global bit-lines can be directly extended to memory output. Only one set of sense amplifiers is required for entire memory so area overhead is reduced.

|  |  |
| --- | --- |
| **Traditional Solution** | **Proposed Solution** |
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**Fig (2.4) Memory data-bus**

**2.3.4 CONCLUSION**

* **Advantages:** Since short bit-lines are used, capacitance offered has decreased. Hence power and delay have reduced.
* **Disadvantages:** Instead of using a single bit-line, number of LBLs and a GBL are being used, due to which area overhead has increased.
  1. **PAPER 3**

**Title:**

Karandikar and K. K. Parhi, *“Low power SRAM design using hierarchical divided bit-line approach,”* in Proc. Int. Conf. Computer Design: VLSI in Computers and Processors, 1998, pp. 82–88.

**2.4.1 OBJECTIVE**

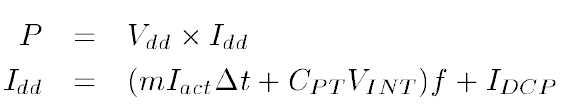
This objective of this paper is to present a novel hierarchical divided bit-line approach for reducing active power in SRAMs by reducing bit-line capacitance.

**2.4.2 INTRODUCTION**

Designing a low power system not only reduces weight and size of batteries for portable systems but also helps in reducing the ever important packaging costs of integrated circuits. To this end, the design of low power digital systems is becoming increasingly important. This paper describes a novel divided bit-line approach for reducing the active power by reducing the bit-line capacitance and then extends it to a hierarchical divided bit-line approach. It is shown that by reducing this capacitance, not only power reduction is achieved but also access time is reduced. Two or more 6T SRAM cells are combined together to divide the bit-line in to several sub bit- lines. These sub bit-lines are again combined to form two or more levels of hierarchy. Optimum values for number of levels of hierarchy and number of blocks combined at each level have been derived.

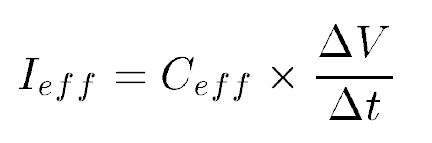
**2.4.3 CONCEPT**

Using a divided bit-line, the delay and power are calculated and power is optimized as follows.

**Eq (2.3)**

**Eq (2.4)**

The total effective charging current flowing during a read operation can be written as



**Eq (2.5)**

Where Ceff is the effective bit line capacitance ∆V is the word line swing and ∆t is word line activation time

The total delay is calculated by

**Eq (2.6)**

Power is calculated by

 **Eq (2.7)**

Power is differentiated with respect to ‘m’ and equated to zero to find an optimal value for ‘m’ (number of cells in a group) which gives minimum power. Since we are trying to optimize delay, an equation for delay, similarly is achieved which is differentiated with respect to ‘m’ and equated to zero to get an optimal value for ‘m’.

**2.4.4 EXPERIMENTAL RESULTS**

A 2K x 8 bits SRAM chip using MAGIC layout tool is designed; 6 and 8 cells are combined at the sub bit-line level.

* Active power consumption has reduced approximately by 50-60%.
* Access time is reduced by 30%.

**2.4.5 CONCLUSION**

* **Advantages:** By dividing bit-line into sub bit-lines, SRAM cells become more stable, as they are guarded from the noise on bit-lines through pass transistors. Active power consumption and access time have decreased.
* **Disadvantages:** Due to hierarchical bit-line setup area overhead increases.

**2.5 SUMMARY**

In this chapter details of literature survey done for this project are discussed. First paper deals with working and design of 4T SRAM and comparison with 6T SRAM in terms of power, area and stability. Second paper deals with delay reduction in SRAM array using buffered bit line technique. This paper gives the basic idea of using divided bit line technique to reduce delay problem in 4T SRAM. Third paper contains concepts related to optimal number of groupings to be done to obtain maximum delay reduction.